WHAT IS CLAIMED IS:

1. A reconfigurable processor, comprising:

a processor core for operating on a set of instructions to carry out predefined processes;

a plurality of input/output pins;

a reconfigurable interface for interfacing between said processor core and said input/output pins, said reconfigurable interface operable to define how each of said plurality of input/output pins interfaces with said processor core and the functionality associated therewith.

2. The reconfigurable processor of Claim 1, wherein said plurality of input/output pins are configured in functional groups.

3. The reconfigurable processor of Claim 1, wherein said processor core has a plurality of inputs/outputs and each of said plurality of said input/output pins can be interfaced with any of said plurality of inputs/outputs of said processor core by said reconfigurable interface.

4. The reconfigurable processor of Claim 1, wherein said reconfigurable interface is programmable by said user.

5. The reconfigurable processor of Claim 1, wherein said processor core is a digital processor core and further comprising an analog section for interfacing via input/output analog pins with analog signals and for interfacing with said processor core with a digital interface.

6. The reconfigurable processor of Claim 5, wherein said input/output analog pins are not reconfigurable with said reconfigurable interface.

7. The reconfigurable processor of Claim 1, wherein said processor core has associated therewith memory.

8. An integrated circuit, comprising:

a processing core for executing a plurality of instructions to carry out a predefined process;

a first memory for containing user defined instructions on which said processing core operates; and

a second imbedded memory for containing proprietary instructions on which said processing core operates and which proprietary instructions are accessible by instructions operating from said first memory, and which second memory is not accessible external to the integrated circuit, said second memory only accessible by instructions in said second memory when executing an instruction therein.

9. The integrated circuit of Claim 8, wherein said first memory is loaded in a first and initializing operation prior to the user programming said second memory and said first memory locked after such loading from access external to the integrated circuit.

10. The integrated circuit of Claim 8, and further comprising a proprietary interface to said first and second memory.

11. The integrated circuit of Claim 10, wherein said first and secnd memories are flash memory.

12. The integrated circuit of Claim 11, wherein said proprietary interface comprises a JTag interface.

13. The integrated circuit of Claim 8, wherein said first memory includes debugging instructions to allow the user to monitor and debug program instructions contained within said second memory, such that the integrated circuit can be operated within its operating environment and debugged therein.